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PATENT

DEPLETION-MODE TRANSISTOR THAT ELIMINATES THE NEED TO SEPARATELY SET THE THRESHOLD VOLTAGE OF THE DEPLETION-MODE TRANSISTOR

This is a continuation of Application Serial No. 09/824,653 filed on April 3, 2001 to Terry Lines. Pat. 6,703,676

BACKGROUND OF THE INVENTION

1. Field of the Invention.

The present invention relates to depletion-mode transistors and, more particularly, to a method of forming a depletion-mode transistor that eliminates the need to separately set the threshold voltage of the depletion-mode transistor.

2. Description of the Related Art.

MOS transistors typically fall into one of two classifications; a depletion-mode transistor or an enhancement-mode transistor. A depletion-mode transistor is a transistor that conducts (more than a leakage current) when the gate, source, and bulk are at the same potential, such as ground for an NMOS transistor and a positive voltage for a PMOS transistor. Depletion-mode transistors are commonly turned off by placing a voltage on the gate that is less than the source voltage for the NMOS transistor, and greater than the source voltage for the PMOS transistor.

An enhancement-mode transistor, on the other hand, is a transistor that is non-conductive (except for leakage currents) when the gate, source, and bulk are at the same potential. Enhancement-mode transistors are commonly turned off by placing ground on the gate of the NMOS transistor and the positive voltage on the gate of the PMOS transistor.

Depletion-mode transistors, in an always-on state, are often used in semiconductor circuits to provide a resistive element. Typically, however, a